CLAIMS

What is claimed is:

1. A substrate imprint tool, comprising:
a light transparent base; and
a light blocking distal end coupled to the light transparent base.

2. The substrate imprint tool of claim 1, further comprises a light transparent neck component formed between the light blocking distal end and the light transparent base.

3. The substrate imprint tool of claim 2, wherein the light transparent neck component to define a trace recess.

4. The substrate imprint tool of claim 2, wherein the light transparent neck component comprises of glass.

5. The substrate imprint tool of claim 2, wherein the light transparent neck component is wider than the light blocking distal end.

6. The substrate imprint tool of claim 1, wherein the light transparent base comprises of glass.

7. The substrate imprint tool of claim 1, wherein the light blocking distal end is to define a via recess.

8. The substrate imprint tool of claim 1, wherein the light blocking distal end further comprises a light transparent core coated with a light blocking material.

9. The substrate imprint tool of claim 1, wherein the light blocking distal end comprises a light transparent core with a bottom surface coated with a light blocking material.

10. The substrate imprint tool of claim 1, wherein the light blocking distal end comprises of a metal.

11. The substrate imprint tool of claim 9, wherein the metal is a selected one of chrome, aluminum, titanium, copper, gold and nickel.

12. A method, comprising:
forming a dielectric layer on a core; and
simultaneously imprinting and at least partially curing a circuitry feature onto the dielectric layer.

13. The method of claim 12, further comprises removing uncured dielectric material from the circuitry feature.

14. The method of claim 13, wherein the uncured dielectric material is a chad.

15. The method of claim 13, wherein the removing of uncured dielectric material from the circuitry feature further comprises dissolving the uncured dielectric material with a solvent that dissolves uncured dielectric material but does not dissolve cured dielectric material.

16. The method of claim 12, wherein the simultaneous imprinting and at least partial curing of circuitry feature further comprises imprinting a via recess.

17. The method of claim 12, wherein the simultaneous imprinting and at least partial curing of circuitry feature further comprises imprinting a trace recess.

18. The method of claim 17, wherein the simultaneous imprinting and at least partial curing of circuitry feature further comprises curing walls of the trace recess.

19. The method of claim 12, wherein the simultaneous imprinting and at least partial curing of circuitry feature further comprises partial UV curing.

20. A package substrate, comprising:
a rigid core;
a dielectric layer formed on the rigid core; and
a circuitry feature formed in the dielectric layer by simultaneously imprinting and partially curing of the dielectric layer.

21. The package substrate of claim 20, wherein the circuitry feature formed in the dielectric layer by simultaneously imprinting and partially curing of the dielectric layer is formed further by using a substrate imprint tool comprising a light transparent base and a light blocking distal end coupled to the light transparent base.

22. The package substrate of claim 20, wherein the circuit component formed comprises a via recess.

23. The package substrate of claim 22, wherein the circuit component formed further comprises a trace recess coupled to the via recess.

24. The package substrate of claim 20, wherein the dielectric material is a crosslinkable polymer dielectric.

25. The package substrate of claim 20, wherein the circuitry feature formed in the dielectric layer by simultaneously imprinting and partially curing of the dielectric layer is further formed by UV partial curing.

26. A system, comprising:
a package substrate, including
a rigid core;
a dielectric layer formed on the rigid core; and

a circuitry feature formed in the dielectric layer by simultaneously imprinting and partially curing of the dielectric layer;

a bus coupled to the package substrate; and

a networking interface coupled to the bus.

27. The system of claim 26, wherein the circuitry feature formed comprises a via recess.

28. The system of claim 27, wherein the circuitry feature further comprises a trace recess coupled to the via recess.

29. The system of claim 26, wherein the dielectric material is a crosslinkable polymer dielectric.